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Development of an Evaluation Platform for Statistical Characterization of MOSFET Model Parameters

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Abstract
In discrete electronics, the statistical variability of device parameters is seldom given in datasheets, at least in such a way that this information can still be useful at design phase. Furthermore, even though several device manufacturers provide simulation models for simulation tools, the device-to-device and lot-to-lot variability of specific parameters is not included in such characterizations, and statistical simulation data is rarely provided, which calls into question the effectiveness of such models. The goal of the present work is twofold. First, it aims to provide a simple but reasonably accurate fitting approach with physical meaning to the static IV curves of long-channel MOSFET transistors. Secondly, it also finds pedagogical purposes, having practical applicability in undergraduate courses of fundamental electronics, as it targets the use of a straightforward approach to derive parameters useful for hand calculations in lab experiments based on experimental data with statistical support.

Subject Headings. Microelectronics, Electrical Engineering, Scientific Education
Author Keywords. Transistor modeling, IV characterization, MOSFET statistical data

1. Introduction

Most well-known circuits relying on MOSFET devices can be explained using some sort of hand-calculation procedures. Such basic understanding is provided by simplified models, which can represent the most relevant physical mechanisms responsible for a certain behavior. However, along with the design process, a reasonable level of accuracy is often required to ensure that the specifications can be met within a given interval of operation conditions. Nonetheless, there is not a simple way to tackle such conflicting requirements, i.e. most professional designers have to deal with the compromises between high accuracy and low complexity almost in a daily basis. On the other hand, from a pedagogical perspective, the large uncertainty in model parameters has a quite negative effect on the learning process for an undergraduate student attending an electronics course. Device manufacturer datasheets provide contained data or occasionally vague, and most of the times the statistical characterization in simulation models is absent. Under such circumstances, a less-experienced designer has extra difficulties on starting to define the values for the circuit components when MOSFET devices are used, leading to abnormal behaviors when such circuits are implemented and tested, which besides being unexpected, are also difficult behaviors to analyze without further information on the MOSFET device.

The present work contributes with a fitting approach to experimental data of MOSFET static operation, providing a simple and simultaneously accurate model that can be used for hand calculations – but without losing physical significance of model parameters. We describe the

development of a complete measurement system, with large amounts of data provided to produce useful statistical information. This paper is organized as follows. Next subsection addresses most fundamental aspects on the static MOSFET modeling, and the following section (Section 2) presents the mathematical background of the proposed fitting technique. Section 3 describes the hardware implementation of the proposed system, Section 4 presents the results, and finally, conclusions are drawn in Section 5.

1.1 MOSFET Static Modeling and Related Issues

With the progressive downscaling of MOSFET devices, short geometries now require the modeling of new phenomena, such as drain induced barrier lowering (DIBL), gate leakage (tunneling), or narrow- and short-channel effects due to interaction of lateral and vertical electrical fields in the channel (Agarwal et al. 2013). In contrast, discrete devices, or MOSFET arrays, typically are built using large and long-channel processes, so such effects denote just a residual influence. However, the Shichman and Hodges (level 1) model is quite inexact in the whole extension of transistor operation, even for large-sized transistors. Still, the level 1 model is vastly delivered in lectures on fundamental electronics, and in almost all textbooks of the field, essentially due to its simplicity. Therefore, although the circuit abstraction in which the model relies is valid (output resistance, transconductance, etc.), the use of a level 1 model is only recommended under very specific (and restricted) operation ranges. Modeling improvements such as the Vladimirescu and Liu model (level 2) have numerical convergence issues, which is tackled in the semi-empirical (level 3) model (Lee 2004). Fitting of the first-generation models mentioned above is not straightforward and the use of too simplistic approaches is not always adequate (Cross and Strickland 2011). The use modified models can help in getting a better understanding on the transistor behavior (Jeppson 2013), but this process requires extreme caution to prevent masking of important effects, such as subthreshold operation or velocity saturation (which is neglected in level 1). Precise characterization can be fully captured using a semiconductor parameter analyzer, capable of an extended MOS parameter extraction (Arora 2007), but not every lab can afford such an expensive instrument. In the present work, we have developed a parameter extraction technique in which a MOSFET level 3 model is used as a basis to achieve a Shichman and Hodges model, to easy obtain the parameters: output resistance ($1/g_{ds}$, or the Early voltage V_A) , device transconductance (g_m) and intrinsic transconductance (K), conduction resistance (g_m), etc. These parameters, together with their statistical information, provide sufficient information for most fundamental designs with MOSFET devices.

2. Proposed Method for Parameter Extraction

For strong-inversion, $V_{GS} > V_{th}$, the current I_{DS} in the SPICE model level 3 is given by (*Synopsys* 2010)

$$I_{DS} = \beta \left[V_{GS} - V_{th} - \tfrac{1}{2}(1 + f_b) V_{DE} \right] V_{DE} \quad (1)$$

with

$$V_{DE} = \min \left\{ V_{DS}, V_{sat} + V_c - \sqrt{V_{sat}^2 + V_c^2} \right\} \quad (2)$$

and

$$V_{sat} = \frac{V_{GS} - V_{th}}{1 + f_b} \quad (3)$$

where f_b is parameter that depends on the geometry and body effect, and V_c is a parameter determined by the carrier velocity saturation as well as the degradation of mobility due to the

lateral electrical field. In triode region, which we will denote as $V_{DS} < V_{sat}$, with V_{sat} provided by (3), we assume $V_c \gg V_{sat}$. This leads to $V_{DE} \approx V_{sat}$, and that way (1) can be rewritten as a function of V_{GS} and V_{DS} as

$$I_{DS} \approx k_1 V_{th} V_{DS} + k_2 V_{DS}^2 + k_3 V_{DS} V_{GS} \quad (4)$$

where the "linear" coefficients k_i are unknown scalars. Let us now assume that V_{DS} and V_{GS} are known, given as column vectors with m and n elements, respectively, i.e. $\vec{v}_{DS} = [v_{DS1}, \dots, v_{DSm}]^T$ and $\vec{v}_{GS} = [v_{GS1}, \dots, v_{GSn}]^T$, with "*T*" implying the transpose operation. Let us also express the matrix $\boldsymbol{P} = \vec{v}_{DS} \times \vec{v}_{GS}$, where "×" means the Cartesian product. This way, one can define

$$\vec{a}_1 = V_{th} \cdot \boldsymbol{P} \cdot \vec{e}_1 \quad (5)$$

$$\vec{a}_2 = \frac{\vec{a}_1 \circ \vec{a}_1}{V_{th}^2} \quad (6)$$

$$\vec{a}_3 = \frac{\vec{a}_1}{V_{th}} \circ (\boldsymbol{P} \cdot \vec{e}_2) \quad (7)$$

where $\vec{e}_i$ represents the *i*-th column of the identity matrix $\boldsymbol{I}_{m \times n}$, and "∘" the Hadamard product. Each of the above resulting column vectors can be used in an $m \times n$ matrix $\boldsymbol{A}$ as follows

$$\boldsymbol{A} = [\vec{a}_1 \quad \vec{a}_2 \quad \vec{a}_3] \quad (8)$$

where the first column denotes all V_{DS} values, repeated n times, the second column is the square of each element of $\vec{a}_1$, and finally the third column is the vector with all possible products between V_{GS} and V_{DS} values. For a data set in which each tuple is obtained from V_{DS} and V_{GS} values, the respective drain current can be written as a column vector $\vec{\imath}_{DS}$. Therefore, one can write

$$\vec{\imath}_{DS} = \boldsymbol{A} \cdot \vec{k} \quad (9)$$

where $\vec{k} = [k_1, k_2, k_3]^T$. As this consists of an overdetermined system certainly with no exact solution because of the nature of experimental (sometimes noisy) data, the least squares estimation can be applied, modifying (9) into a normal equation, i.e. $\boldsymbol{A^T} \cdot \vec{\imath}_{DS} = \boldsymbol{A^T} \cdot \boldsymbol{A} \cdot \vec{k}$. Therefore, if $\boldsymbol{A^T} \cdot \boldsymbol{A}$ is invertible, it is possible to find a solution for the least-squares problem, which coincides to finding the values of $\vec{k}$ that minimize the norm of residuals, i.e. $\left\| \vec{\imath}_{DS} - A \cdot \vec{k} \right\|^2$.

The validity of the model using (4) is limited to the triode region, i.e. saturation, cutoff and weak inversion cannot be included for the purpose of finding $\vec{k}$. But, that leads to another problem, which is finding V_{sat} since both V_{th} and f_b are unknown parameters. The parameter V_{th} is extracted by linear extrapolation of $I_{DS}(V_{GS})$ at the point of maximum slope (Ortiz-Conde et al. 2013). However, f_b would still be unknown. As in practice, typically the design bias point is arbitrated either in saturation or triode, one way is to first define a region far from the transition, such as $V_{DS} < (V_{GS} - \hat{V}_{th})/(1 + \hat{f}_b)$, where $\hat{V}_{th}$ is the threshold voltage estimated by the linear extrapolation, and $\hat{f}_b$ is the parameter used to initially define the triode region under consideration (in the order of 1). A first fitting will provide $-k_1 = \beta$ and $k_2/k_3 = -(1 + f_b)/2$.

It is important to note that f_b is essential to correctly define the triode region. In the Shichman and Hodges model this parameter is null. However, even in the long-channel case the pinch-

off voltage given by $V_{DS} = V_{GS} - V_{th}$ leads to a substantial error. Figure 1 provides an example for a long-channel NMOS in which $\hat{f}_b$ is swept to identify different triode-saturation transitions. Note that for a null $\hat{f}_b$ the triode gets into what is interpreted by already deep saturation by visual inspection, thus leading to complete different results. Hence, even for long and wide channels, as seen here, the use of a level 3 model is completely justified. It should be mentioned also that for our purpose, the estimation of this parameter ($\hat{f}_b$) only gives a region, which under such consideration allows us to obtain the "true" value of f_b.

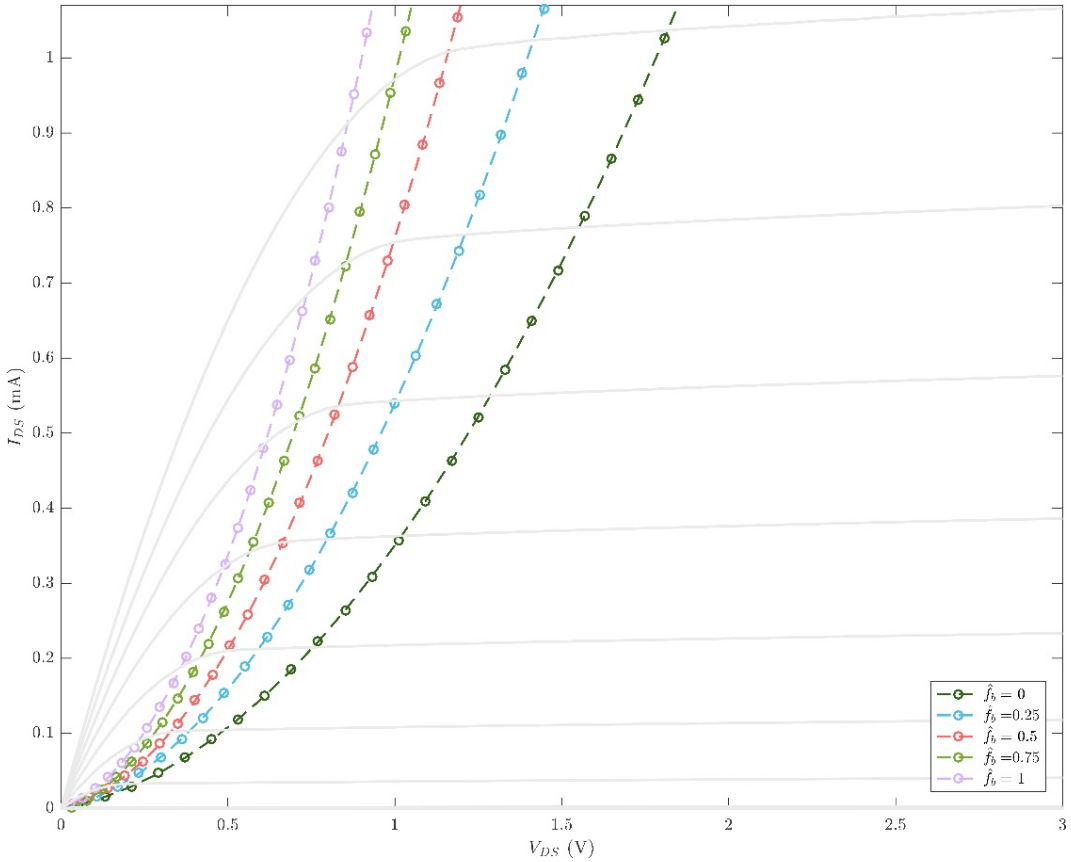

Figure 1: Transitions obtained between triode and saturation regions, defined according to the parameter $\hat{f}_b$ (with $\hat{V}_{th}$ fixed) for a long- and wide-channel device ($W/L = 138.0\mu$m/8.0μm)

In saturation, we will consider V_{DS}>V_{sat}, with V_{sat} provided by (3). We will assume that $V_c \gg V_{sat}$, which leads to $V_{DE} \approx V_{sat}$, and that way (1) can be rewritten as an approximate function of V_{GS} as follows

$$I_{DS} \approx \frac{1}{2}\beta \frac{1}{1+fb}(V_{GS} - V_{th})^2 \quad \textbf{(10)}$$

However, in the saturation regime, the equations for model level 3 first lead to a value of I_{DS} without channel modulation, and only its influence is determined, by affecting the original value of I_{DS} by a dependence on V_{DS}. In our case, we will depart from (10) and introduce channel length modulation by introducing a factor $1 + \lambda V_{DS}$, i.e.

$$I_{DS} \approx u_1 V_{th} V_{GS} + u_2 V_{GS}^2 + u_3 V_{th}^2 + u_4 V_{GS} V_{DS} + u_5 V_{GS}^2 V_{DS} V_{th} + u_6 V_{DS} V_{th}^2 \quad \textbf{(11)}$$

still approximated by

$$I_{DS} \approx w_1 V_{GS} V_{th} + w_2 V_{GS}^2 + w_3 V_{th}^2 + w_4 V_{GS}^2 V_{DS} \quad \textbf{(12)}$$

For the determination of u_i coefficients, we will use the values of f_b and V_{th} derived earlier, so that the saturation region is well defined, and the right amount of points can be used. To

derive a least squares formulation, we reuse $\boldsymbol{P}$ as given before, and now define the column vectors

$$\vec{a}_1 = V_{th} \cdot \boldsymbol{P} \cdot \vec{e}_2 \quad (13)$$

$$\vec{a}_2 = \frac{\vec{a}_1 \circ \overrightarrow{a_1}}{V_{th}^2} \quad (14)$$

$$\vec{a}_3 = V_{th}^2 \cdot \vec{1} \quad (15)$$

$$\overrightarrow{a_4} = \overrightarrow{a_2} \circ (\boldsymbol{P} \cdot \vec{e}_1) \quad (16)$$

and the matrix $\boldsymbol{A}$

$$\boldsymbol{A} = [\vec{a}_1 \;\; \vec{a}_2 \;\; \vec{a}_3 \;\; \vec{a}_4] \quad (17)$$

Hence, the previous approach to determine (9) can be used to obtain $\vec{w} = [w_1 \; w_2 \; w_3 \; w_4]^T$, instead of $\vec{k}$. Fig. 2 exemplifies the results for fitting the saturation region from the method described above (red circles). If we use $w_4 = 0$ in (12) and compute again w_1 , we obtain the representation given in Fig. 2 denoting no channel length modulation (blue squares in figure).

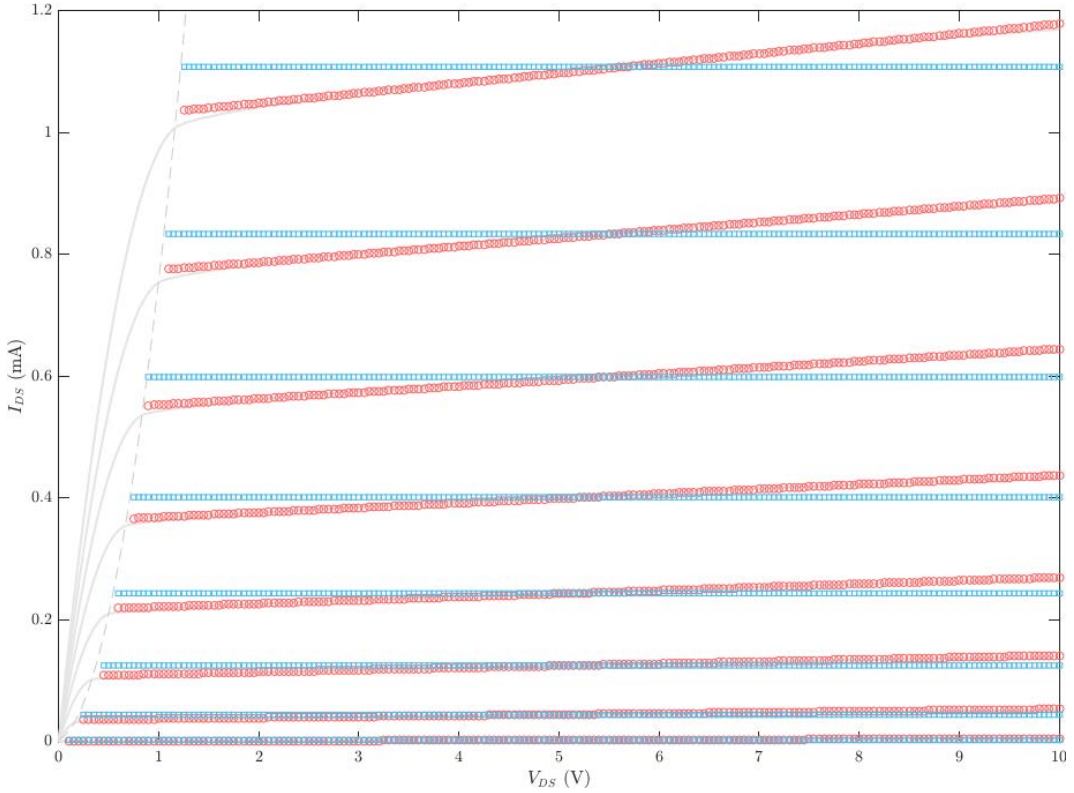

Figure 2: Fitting for the saturation region considering (red circles) and neglecting (blue squares) channel length modulation

For a quick parameter list of the Shichman and Hodges model, $I_{DS} = K(V_{GS} - V_{th})^2(1 + V_{DS}/V_A)$ in region $V_{DS} \gg V_{GS} - V_{th} \gg 0$, we can use the results obtained and, around a specific point $(V_{DS}; I_D)$, determining K and V_A as

$$K \approx w_2 \quad (18)$$

From (12), at the desired point $(V_{DS}; I_D)$, the remaining bias value V_{GS} is derived, and then applying $\partial I_D/\partial V_{DS}$ at that point, one can also attain $V_A = I_D \cdot (\partial I_D/\partial V_{DS})^{-1}$. The value of g_m is obtained with $\partial I_D/\partial V_{GS}$, see eq. 19, for the V_{DS} arbitrated.

$$g_m \overset{\text{def}}{=} \frac{\partial I_D}{\partial V_{GS}} = w_1 V_{th} + 2w_2 + 2w_4 V_{DS} V_{GS} \quad (19)$$

3. System Implementation

The proposed system was implemented as a mezzanine approach, i.e. with a raspberry-pi zero mounted on top of a PCB designed for the present purpose, in which all circuits have been employed. Fig. 3 depicts a photograph of the hardware developed, with the main PCB just mentioned and two examples boards in which the device under test (DUT) is attached to. The raspberry and the DUT boards make use from the power supply of the main board, with two dc power levels, 5V and 12V, obtained with linear regulators, i.e. LM1085IT/05 and /12NOPB, respectively, both from Texas Instruments (minimum limit of 3.2A).

The *raspbian* (Debian based) distribution is employed in the raspberry, and python scripts are used to control the hardware. The use of a flat cable allows different DUTs to be tested. Two of the flat cable wires are used in open or short-circuit at the DUT board to identify which DUT is being connected – those lines are read at an analog-to-digital (ADC). At each DUT board there is a pushbutton to start a new set of measurements, to which a counter is associated to display (with two seven-segment digits) a number for each measurement.

At the raspberry, the data is stored in a 8-GB SD card as plain text files (in a CSV format). There is an Apache server, with PHP modules, which allows the data to be displayed to a user in a local area network, to provide the file download with all the measurements, as well as the fitting data. For internet connection, the raspberry is connected via microUSB to a hub with an Ethernet connection and extra USB ports (used for debugging purposes, i.e. connect to a display and mouse).

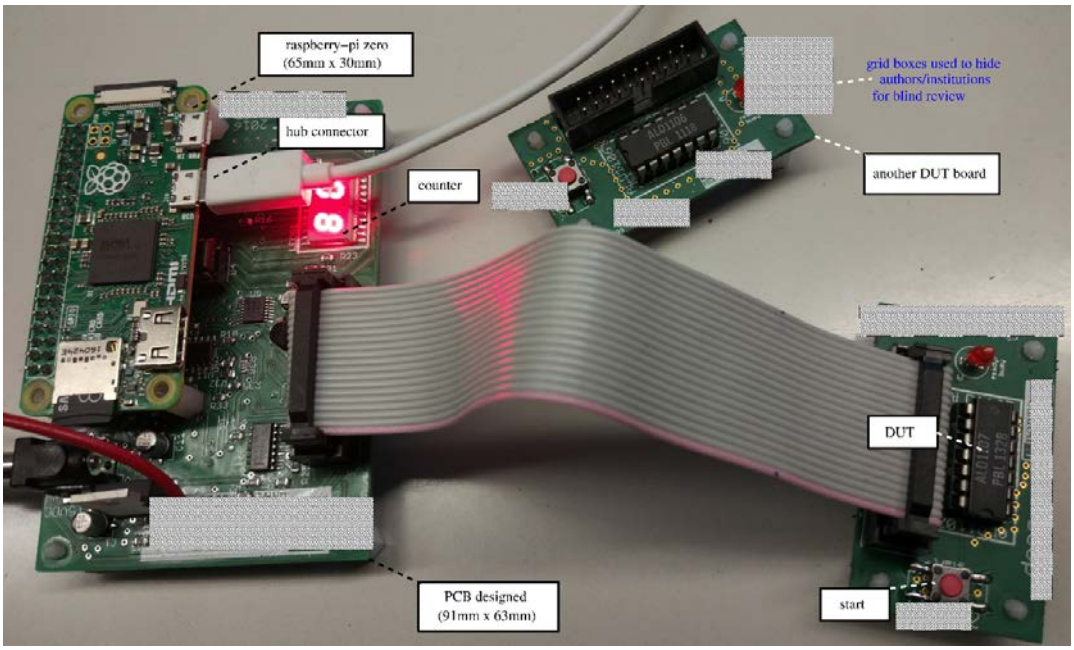

Figure 3: Hardware implementation

Fig. 4 depicts the circuits used to measure the current flowing through the DUTs. The board is prepared to test 4 DUTs (usually an array of matched transistors) in a single integrated circuit. The MOSFET arrays used as DUTs in this work are N channel devices, ALD1106 (the system is also prepared for ALD1107), from Advanced Linear Devices Inc – this device is used in electronic lab classes in numerous universities across USA, e.g. Berkeley, UC Santa Barbara, etc.). Two dual DACs are used (AD5697, 12bit, from Analog Devices) to provide the drain, gate, and source voltages. A Delta-Sigma ADC with 4 channels is employed to sense the current (ADS1115, 16 bit, Texas Instruments) using the scheme provided in Fig. 4 – both the ADC and

DAC use I2C for communication with the raspberry, with the SDA and SCL signals connected to the GPIOs of the raspberry.

The two different power levels imply that the buffering employs half-voltage reduction (in sensing) and voltage doubling (in driving) between ADC and DACs. Precision (75uV offset) rail-to-rail opamps are used to this end (quad opamp, OPA4180, from Texas Instruments) having low typical offset drift with temperature (0.1µV/ºC), and resistors in SMD package with maximum error of 0.1%. In the present case of Fig. 4, the resistors are made all equal, i.e. $R_{M11} = \cdots = R_{M42} = R_{D11} = \cdots = R_{D42} = R_{S11} = \cdots = R_{S41} = R = 10\,\mathrm{k}\Omega$, except for the resistors in which the current is sensed, i.e. $R_{i1} = \cdots = R_{i4} = R_i = 110\,\Omega$. The current is obtained indirectly from

$$I_{DS} = 2\frac{\tilde{V}_M - \tilde{V}_D}{R_i} - \frac{\tilde{V}_D}{R} \tag{20}$$

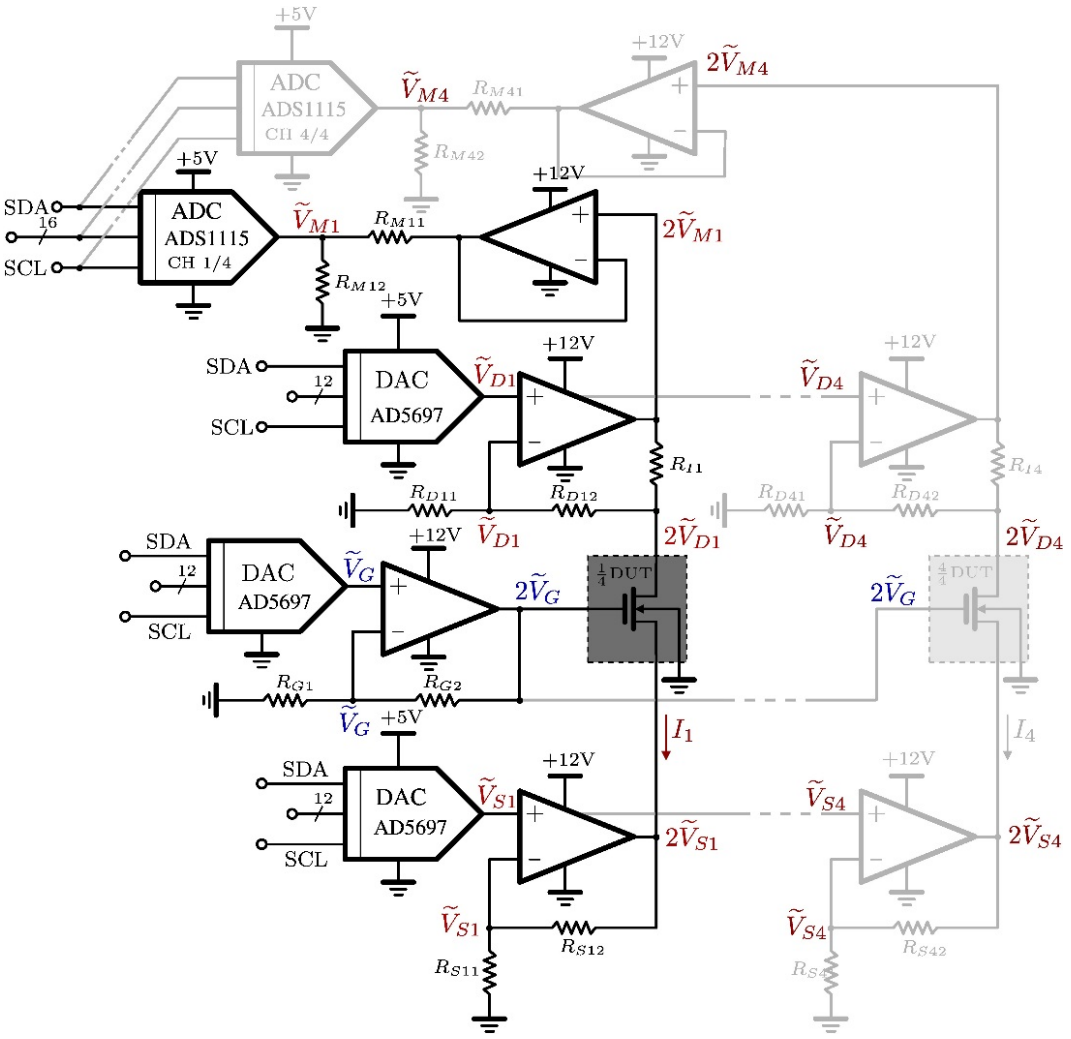

Figure 4: Circuits for I_{DS} sensing (the ground connection at the DUT can be replaced by a positive voltage connection depending on the DUT board used)

The voltage offsets and voltage gain have been measured with a 6 1/2-digits multimeter (Keysight 43310A). The offsets measured for the acquisition chain are, in average for all four channels, in the order of 1.6 mV (-923 µV in the opamp+DAC chain and 2.5mV at the ADC), whereas the maximum slope error measured is about 0.6%. These values do not compromise the integrity of the measurements and are quite low to bias the results for different devices. The time to obtain a $I_{DS} - V_{DS}$ measurement with the ALD1106 is about 57 seconds, for the 4

transistors (for a measurement with PMOS devices it takes less time, about 1/3, because the voltage values to impose are due to different DACs).

4. Results

The developed platform was tested with 73 samples from MOSFET arrays ALD1106, each having 4 N-channel transistors. These devices are from 6 distinct lots (denoted here as A to F). Figure 5 depicts the histogram for three parameters extracted (V_{th}, K, and V_A). The parameters K was obtained from(18) and V_{th} was obtained from linear extrapolation, extracting $\frac{V_{DS}}{2}$. For the Early voltage, a current of 575 µA has been arbitrated, for V_{DS} of 2.5V (see Fig. 6). It is interesting to note that, although V_A is almost unchanged, the remaining parameters show a great difference when the devices are from different lots, implying bimodal distributions – also devices with defects are included in data. Table 1 summarizes all statistical information.

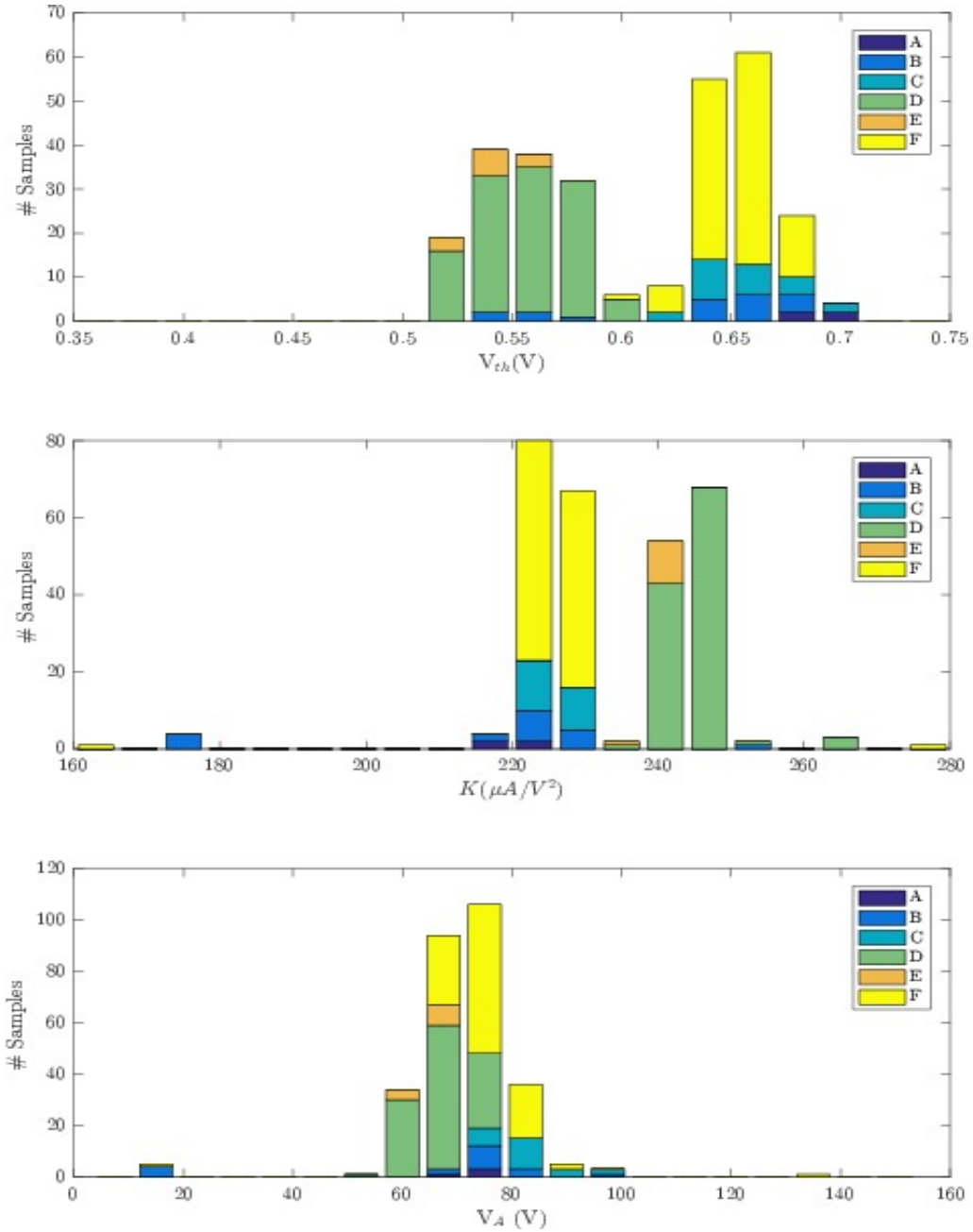

Figure 5: Histogram of extracted parameters V_{th}, K, and V_A

Parameter	Mean	Standard deviation	Units
V_{th}	0.609	0.0531	V
K	233.56	12.535	µA/V^2
V_A	67.39	10.752	V
g_m	0.746	0.023	mA/V
I_{DS}	574.96	0.017	µA

Table 1: Summary of the extracted parameters for all the devices (all lots together) with the target current I_{DS} =575µA, V_{DS} = 2.5V

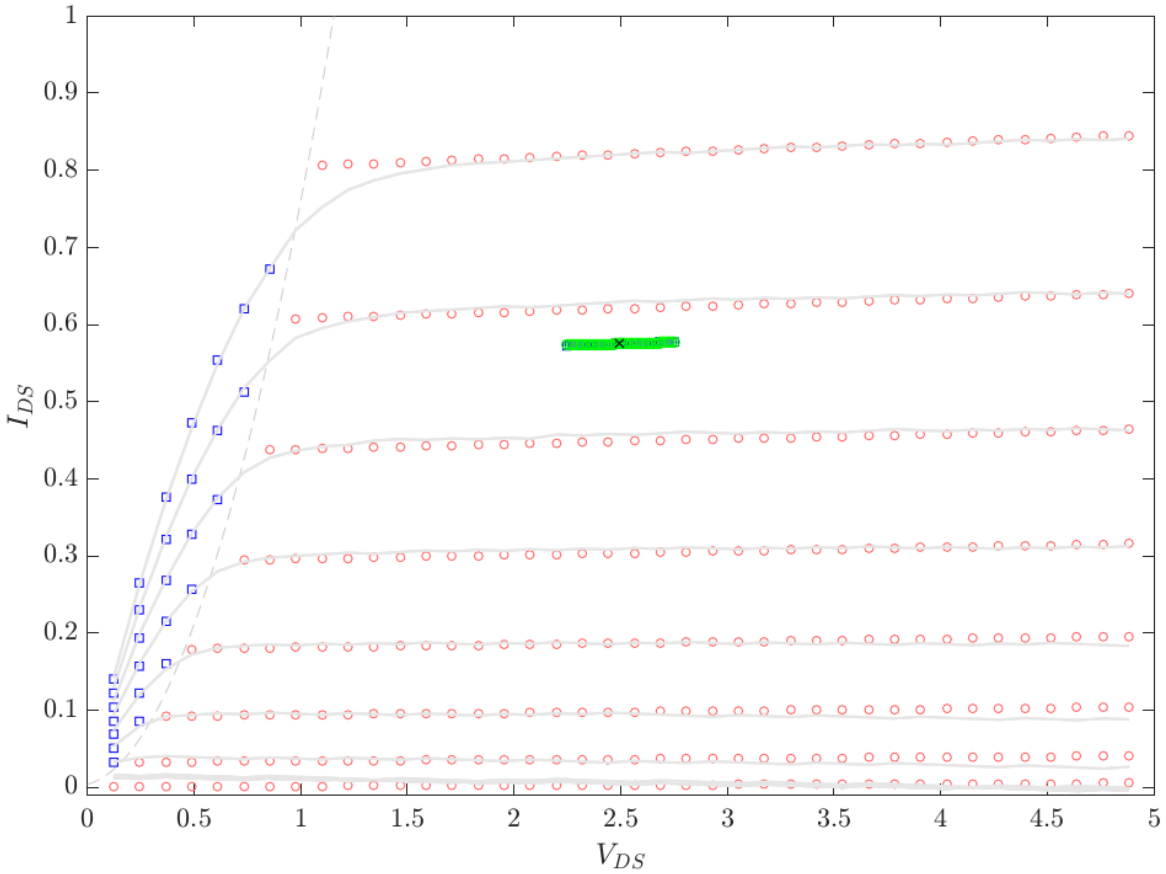

Figure 6: First-order approximation for $I_{DS} = 575\mu$A and $V_{DS} = 2.5$V (black ×) for a random device; the green circles denote the point vicinity with constant V_{GS}; the remaining symbols are from the polynomial approximations in triode and saturation, whereas the gray lines are from the actual measurement

To test the extracted parameters, two circuits have been implemented, as shown in Fig. 7. The common source circuit in Fig. 7 (a) leads to an experimental gain of about -2.7V/V (see Fig. 8), which means a minor deviation (around 7%) from the predicted ($g_{m2} = 773\mu\text{A/V}$, $r_{o2} = 121\text{k}\Omega$, hence $A_v = -2.9$ V/V). In the circuit with unitary gain, i.e. Fig. 7(b), the output resistance obtained was 1251Ω, which is about 8% of the calculated value ($g_{m3} = 723\mu\text{A/V}$, $r_{o2} = 128\text{k}\Omega$).

$g_{m2} = 773\mu\text{A/V}, r_{o2} = 121\text{k}\Omega,$

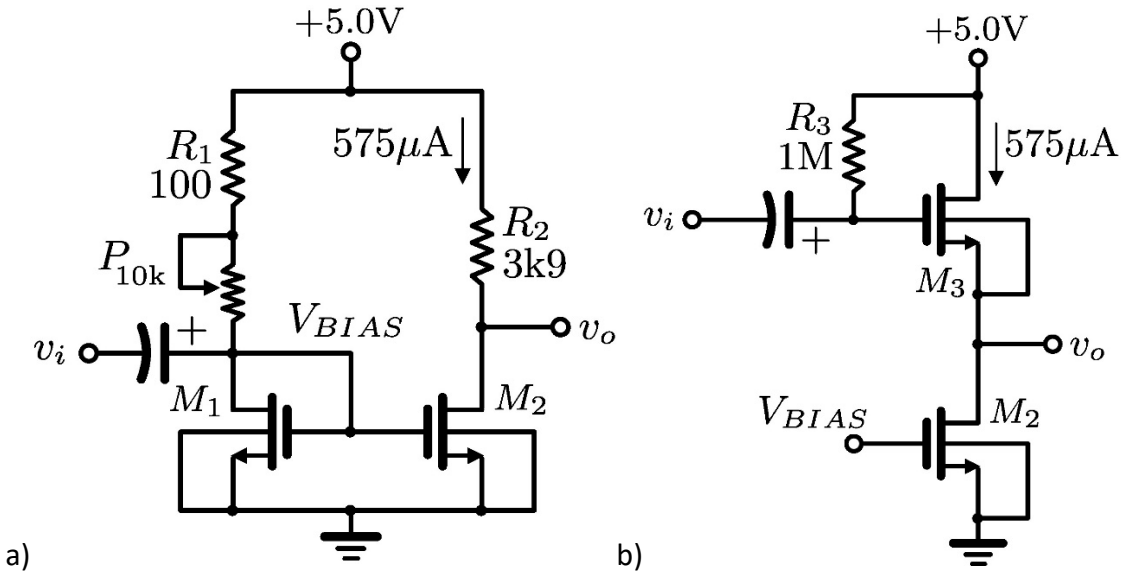

Figure 7: Circuits for testing extracted signal parameters

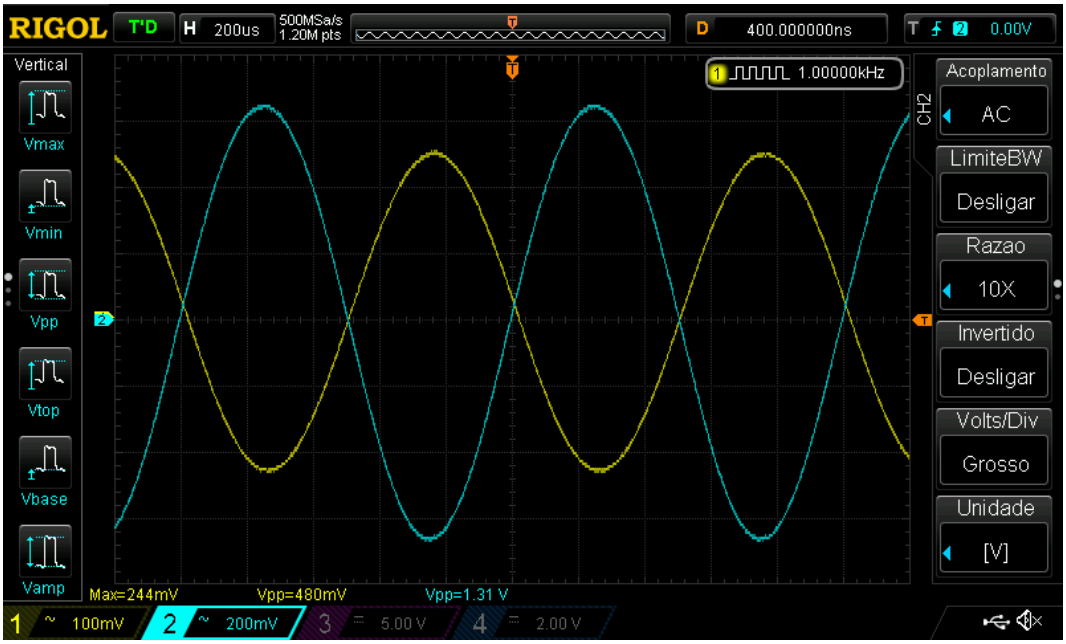

Figure 8: Input and output voltages in the circuit Fig. 7(a)

5. Conclusions

We describe the study and development of a characterization platform suitable for parameter extractions of MOSFETs with a system capable of measuring the dc behavior of MOSFETs, providing the measured data online in a local area network, storing and processing statistical information. Furthermore, we provided the model fitting of most relevant parameters for hand calculations.

The proposed platform has been tested and validated with NMOS arrays. This work finds an adequate use in courses of fundamental electronics, with the potential of improving both the interest and learning of undergraduate students in analog electronics. It tackles most difficulties when dealing with MOSFET circuits, when approximating the static behavior to the most simplistic approach (level 1) during design, i.e. when there is no further insight on the complete characteristics of the active device. The use of the provided level 1 model, approximated in the vicinity of a target bias point, allows better predictability. Furthermore,

it allows its use in conjugation with the parameter statistics provided by the proposed platform. Future work would include validation of these models when applied to small-signal operation in analog circuits.

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