

Design of Low Voltage Low Power High Gain Operational Transconductance Amplifier

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Abstract

In this paper, a high gain structure of operational transconductance amplifier is presented. For low voltage operation with improved frequency response bulk driven quasi-floating gate MOSFET is used at the input. Further for achieving high gain the modified self cascode structure is used at the output. Compared to conventional self cascode the modified self cascode structure used provides higher transconductance which helps in significant boosting of gain of the amplifier. The modification is achieved by employing quasi-floating gate transistor which helps in scaling of the threshold which as a result increases the drain-to-source voltage of linear mode transistor thus changing it to saturation. This change of mode boosts the effective transconductance of self cascode MOSFET. The proposed operational transconductance amplifier when compared to its conventional showed improvement in DC gain by 30dB and also the unity gain bandwidth increases by 6 fold. The MOS models used for amplifier design are of 0.18 μ m CMOS technology at supply of ± 0.5 V.

Author Keywords. Self Cascode, Quasi-floating Gate, Transconductance, Current Mirror, OTA, Gain, Bandwidth.

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1. Introduction

The deep submicron device dimensions and low voltage operations have favoured the design of high performance circuits. However, encouraging results were not achieved in case of analog circuits. The reason is the presence of channel length modulation (CLM) effect. To overcome this in literature different techniques have been adopted but the widely accepted is self cascode (SC) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) structure (Galup-Montoro, Schneider, and Loss 1994; Gerosa and Neviani 2003). Besides the advantage of SC MOSFET, it does suffer with a disadvantage in terms of requirement of large device dimensions. Solutions in this context include using MOSFET of asymmetric threshold voltage (V_{th}) (Fujimori and Sugimoto 1998), MOSFET with dual-work function-gate (DWFG), zero threshold (ZVT) MOSFET (Na, Baek, and Kim 2012), body-biasing technique (Baek et al. 2013) etc. But these solutions require complicated fabrication processing steps (Baek, Kim, and Kim 2016). In low voltage circuits, the threshold voltage has continuously forced analog designers to struggle in order to meet the circuit specifications. The reason is that the minimum supply voltage cannot be scaled below the threshold voltage of MOSFET. Few widely adopted low voltage (LV) low power (LP) non-conventional techniques reported in literature include Bulk Driven technique (Blalock, Allen, and Rincon-Mora 1998), Floating Gate (FG) structure (Hasler and Lande 2001), Quasi-floating Gate (QFG) structure (Ramirez-Angulo et al. 2003; Ramirez-

Angulo et al. 2004), and Bulk driven floating/quasi-floating Gate (BDFG/BDQFG) structure (Khateb 2014, 2015). Among the aforementioned techniques BD is chosen for very LV operation but it does suffer from low transconductance for which the BDQFG technique is preferred over it. Also, in these non-conventional techniques transconductance achieved is low compared to standard gate driven MOSFET which leads to low bandwidth circuits. In this paper, a modified structure of gate driven SC is proposed which uses the QFG MOSFET. The proposed structure offers enhanced transconductance which can be used in design of any LV analog circuits for further circuit performance improvement.

The paper is divided in five sections. Following the introduction made on Section 1, Section 2 details about the proposed QFG-SC structure followed to realization of circuits based on proposed QFG-SC in section 3. This includes current mirror circuits and operational transconductance amplifier (OTA) realization. The simulation results are discussed in section 4 followed to conclusion in section 5.

2. Self Cascode Structure

A modified structure of SC based on QFG MOSFET is proposed in this section. Figure 1(a) and Figure 1(b) are the conventional and proposed QFG-SC structures.

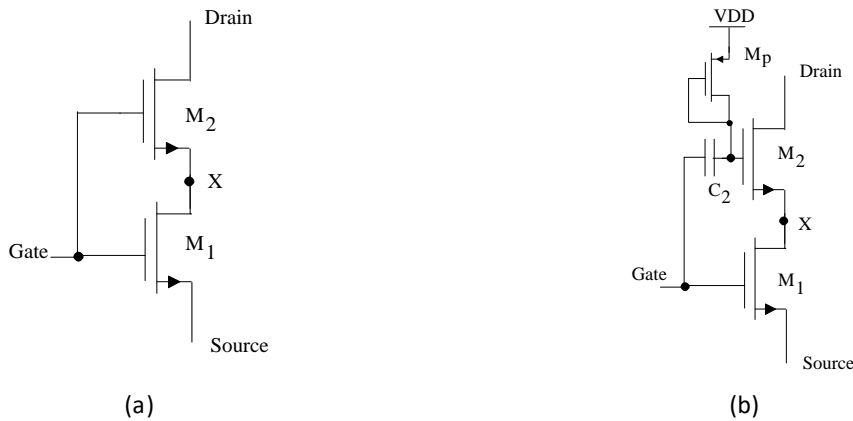


Figure 1: Self cascode structure: (a) Conventional SC; (b) Modified QFG-SC

Here in Figure 1(a), M₁ operates in linear mode whereas M₂ in saturation mode. As known the transconductance achieved is maxima when MOSFET operates in saturation so by changing M₁ to saturation mode the effective transconductance of the SC structure can be enhanced which can be used in design of high gain circuits. If $V_{th,M2} < V_{th,M1}$ is achieved then a possibility to increase V_{DS} of M₁ can be achieved. The necessary condition required to be satisfied for operating both the MOSFETs of SC in saturation region is:

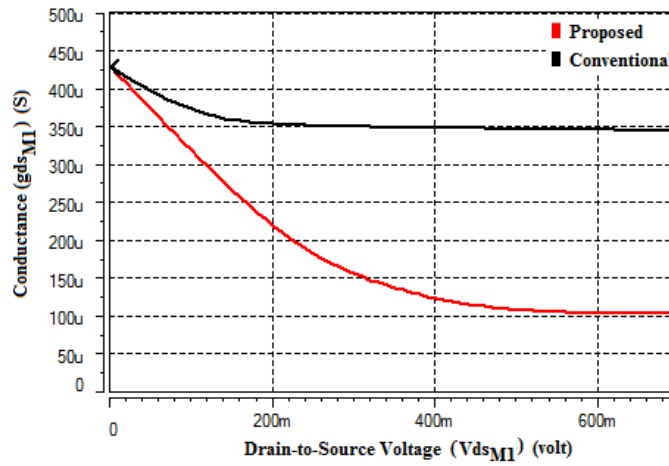
$$V_{DS,sat.M2} \geq V_{th,M1} - V_{th,M2} \tag{1}$$

To satisfy the condition of (1), QFG is used in the proposed SC design as shown in Figure 1(b) where MOSFET M₂ is converted into QFG MOSFET. The effective threshold voltage of M₂ changes to

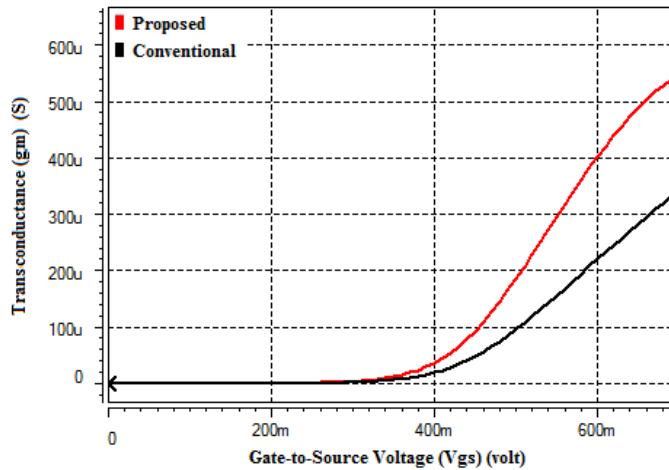
$$V_{th2,eff} = \frac{C_{T,qfg}}{C_2} V_{th2} - \frac{C'_{GD,MP}}{C_2} V_{DD} \tag{2}$$

where $C_{T,qfg}$ is the total capacitance seen at the QFG node of M₂ and $C'_{GD,MP}$ is the parasitic capacitance of M_p. The capacitor C₂ and MOSFET M_p is used to realize M₂ in QFG mode. As seen in (2), the effective threshold of M₂ gets scaled down which increases the possibility of satisfying the condition of (1) and the MOSFET M₁ enters into saturation. This result in rise in effective transconductance which is given as:

$$G_{m,QFG-SC} = \frac{g_{m1}r_{01} + g_{m2,qfg}r_{02,qfg} + g_{m1}g_{m2,qfg}r_{01}r_{02,qfg}}{r_{01} + r_{02,qfg} + g_{m2,qfg}r_{01}r_{02,qfg}} \quad (3)$$



(a)



(b)

Figure 2: Simulation: (a) Output conductance of M₁; (b) Transconductance

The output conductance of M₁ MOSFET and effective transconductance plot of self cascode (Figure 1) are shown in Figure 2(a) and Figure 2(b) respectively. The MOS model used is of 0.18μm technology and simulation has been done by applying 1V supply at drain terminal and the source terminal is connected to ground. At gate-to-source voltage of 0.6V, in proposed QFG-SC the output conductance of M₁ becomes threefold smaller whereas the overall transconductance gets doubled when compared to its conventional design. So, it can be stated that by employing the proposed structure the performance of analog circuits can be easily enhanced for example in current mirrors (Raj et al. 2014a, 2014b, 2015; Raj 2021; Doreyatim et al. 2019; Bchir, Aloui, and Hassen 2020), where the transconductance decides the performance parameter.

3. Proposed QFG SC based OTA

The current mirror based OTA (Allen and Holberg 2002) based on BD approach for low voltage operation is shown in Figure 3(a). It uses three current mirror topologies. These three current mirror combinations are (M3, M5), (M4, M6) and (M7, M8) whereas combination (M9, M10) forms a current mirror for biasing the OTA using a constant current source (I_{bias}).

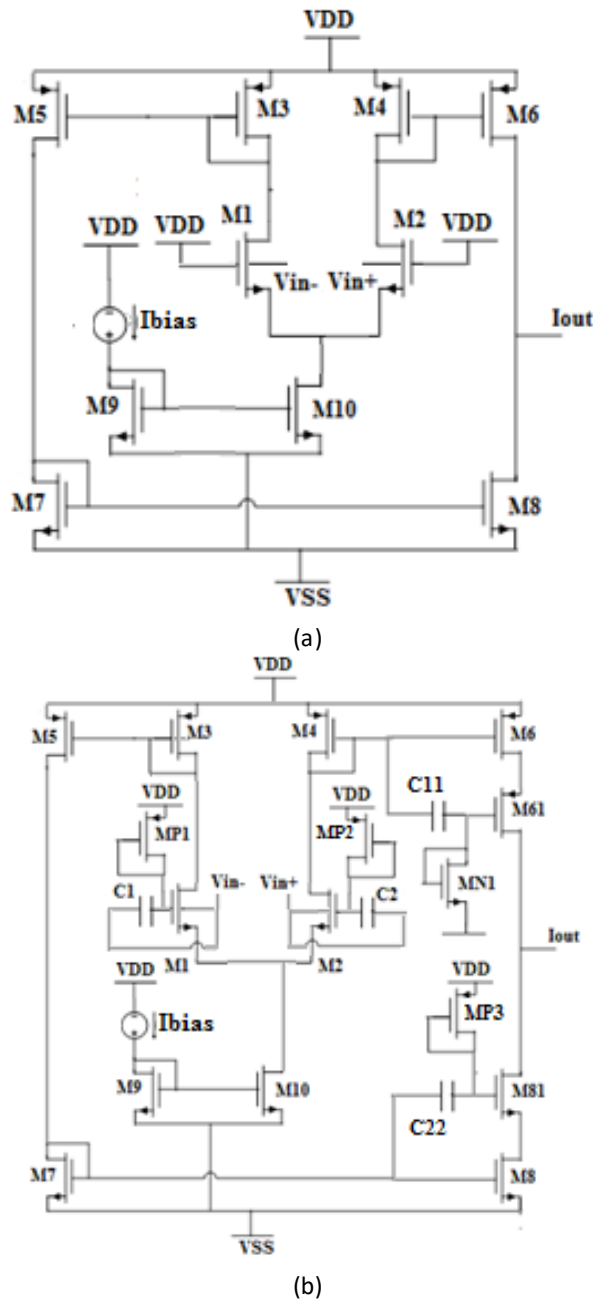


Figure 3: OTA (a) Conventional BD OTA; (b) Proposed BDQFG QFG-SC OTA

The design equations governing the OTA performance parameters of Figure 3 are:

(i) Transconductance,

$$G_m = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_2} I_{10} \tag{4}$$

(ii) Output Resistance,

$$R_{out} = 1/(g_{ds6} + g_{ds8}) \tag{5}$$

(iii) DC gain,

$$A_v = G_m R_{out} = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_2} I_{10} \left(\frac{1}{g_{ds6} + g_{ds8}}\right) \tag{6}$$

(iv) Dominant pole,

$$\omega_{-3dB} = 1 / (1/g_{ds6} + g_{ds8}) C_L \tag{7}$$

(v) Unity-gain bandwidth,

$$UGB = \frac{G_m}{C_L} = \left(\sqrt{\mu_n C_{ox} \left(\frac{W}{L} \right)_2 I_{10}} \right) / C_L \tag{8}$$

Due to low transconductance of input MOSFETs (M1 & M2), the achieved gain is of low value. In context to this, the BD is replaced by BDQFG MOSFET which improves the performance. Also from (6), it can be observed that the DC gain of the amplifier can be improved by reducing the g_{ds} of transistors M6 and M8. Keeping in view the DC gain, transistor M6 and M8 is replaced by proposed QFG-SC structure as shown in Figure 3(b). Here pair (M6, M61) forms a P-type QFG-SC structure where M61 is configured in QFG mode using capacitor C11 and cut-off mode transistor MN1. Similarly, pair (M8, M81) forms N-type SC structure where M81 is configured in QFG mode using capacitor C22 and cut-off mode transistor MP3. The overall DC gain of the amplifier increases due to decrease in the magnitude of conductance of output transistors.

4. Simulation Results

The conventional and proposed OTA are simulated on 0.18µm twin-well CMOS process at ± 0.5 V power supply with the help of Spice simulator under the same environment. The enhancement type of MOSFETs is used in this paper to design the circuits. The MOS transistor device dimensions taken for simulation purpose for CM OTAs of Figure 3 are shown in Table 1 along with other assumed parameters for circuit simulations.

The effective transconductance plot for OTA under different configuration is shown in Figure 4. From the plots it can be observed that for BD OTA effective transconductance is 12.9uA/V whereas when OTA is modified using BDQFG and SC the effective transconductance becomes 50.8uA/V which further gets boosted to 87.5uA/V by employing QFG-SC structure. As the OTA transconductance gets boosted it results in increased DC gain as well the unity gain frequency.

Transistors	Width (µm)	Length (µm)	Transistors	Width (µm)	Length (µm)
M1	15.12	1.26	M8	15.12	1.26
M2	15.12	1.26	M81	15.12	1.26
M3	15.12	1.98	M9	15.12	1.98
M4	15.12	0.72	M10	15.12	1.98
M5	15.12	1.98	MP1	0.24	0.24
M6	15.12	0.72	MP2	0.24	0.24
M61	15.12	0.72	MP3	0.24	0.24
M7	15.12	1.26	MN1	0.24	0.24

C1=C2=C11=C22=1pf, CL=1pf, supply= ± 0.5V, I_{bias}=10uA

Table 1: W and L of MOSFET used in conventional and proposed OTA

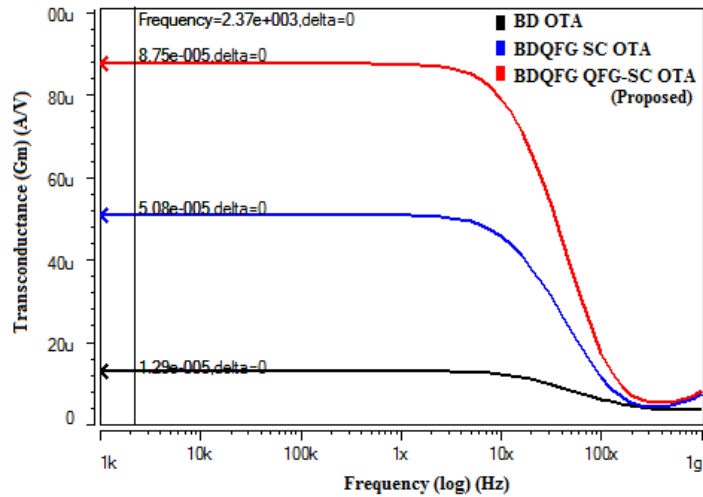


Figure 4: Transconductance plots

The DC gain plots for conventional OTA and proposed QFG-SC OTA are shown in Figure 5. The observed improvement in DC gain by QFG-SC OTA is by 30dB, i.e. gain increases from 20dB to 50dB. Also improvement is seen in unity gain bandwidth which for the proposed OTA is 12MHz whereas for conventional is 2MHz. The transient response is shown in Figure 6 where the BDQFG QFG-SC OTA tracks the input fast with minimum offset. From the simulation results it can be easily concluded that using QFG-SC in any low voltage circuits can result in high performance as compared to simple SC structure. The performance analysis of OTA's as obtained by simulations is summarized in Table 2.

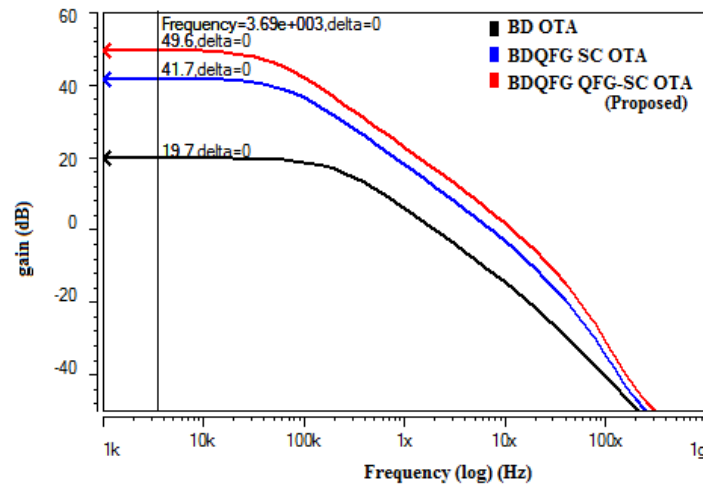


Figure 5: Gain plots

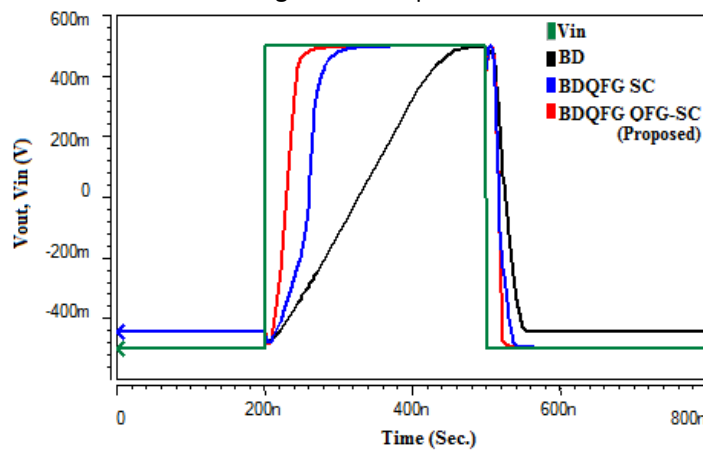


Figure 6: Transient plots

Parameters	BD	BDQFG SC OTA	BDQFG QFG-SC OTA (Proposed)
Transconductance (Gm) (uA/V)	12.9	50.8	87.5
DC gain	19.68	41.71	49.61
F3db (KHz)	208.65	65.28	45.66
UGB (MHz)	2	7.45	11.96
Phase Margin (PM)	91.17	67.49	55.45
Power (uW)	20.79	21.41	23.44
Voltage Supply	± 0.6V	± 0.5V	± 0.5V

Table 2: Performance analysis of OTA

5. Conclusion

A high performance design of OTA using modified SC structure has been proposed where the improvement achieved is in terms of DC gain as well unity gain bandwidth. For low voltage operation BDQFG technique has been used as with BD there is drawback of poor transconductance. The output section when modified with SC boosted the gain which further got boosted by QFG-SC structure. The achieved DC gain and unity gain bandwidth and high speed encourages it application in high performance VLSI design.

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